

## CLAIMS

Therefore, having thus described the invention, at least the following is claimed:

1           1.       An apparatus for use in a computer graphics system, comprising:  
2           a plurality of depth buffers for storing depth data, wherein at least one of the  
3           plurality of depth buffers is configured to provide depth data for a group of pixels,  
4           wherein at least one other of the plurality of depth buffers is configured to provide depth  
5           data for each pixel of the group;  
6           a plurality of stencil buffers, the stencil buffers configured to store stencil shadow  
7           volume data, wherein at least one of the plurality of stencil buffers is configured to  
8           provide stencil shadow volume data for the group of pixels; wherein at least one other of  
9           the plurality of stencil buffers is configured to store stencil shadow volume data for each  
10          pixel of the group; and  
11          control logic for controlling the plurality of stencil buffers and the plurality of  
12          depth buffers, wherein the stencil shadow volume data is generated and stored.

1           2.       The apparatus of claim 1, wherein the plurality of depth buffers comprise:  
2           a first depth buffer, wherein the first depth buffer has a plurality of first depth  
3           buffer records, such that each first depth buffer record stores depth data for a group of  
4           pixels, where the group of pixels comprises a tile; and  
5           a second depth buffer, wherein the second depth buffer has a plurality of second  
6           depth buffer records, wherein each second depth buffer record stores depth data for a  
7           pixel.

1           3.       The apparatus of claim 2, wherein the plurality of the stencil buffers  
2 comprise:

3           a first stencil buffer, wherein the first stencil buffer has a plurality of first stencil  
4 buffer records, such that each first stencil buffer record stores the stencil shadow volume  
5 data for the tile; and

6           a second stencil buffer having a plurality of second stencil buffer records, such  
7 that each second stencil buffer record stores the stencil shadow volume data for each  
8 pixel, wherein the second stencil buffer record is configured as a partition of the second  
9 depth buffer record.

1           4.       The apparatus of claim 3, further comprising:

2           a first cache, wherein the first cache is configured to communicate data with the  
3 first depth buffer; wherein the first cache is further configured to communicate data with  
4 the first stencil buffer; and

5           a second cache, wherein the second cache is configured to communicate data with  
6 the second depth buffer, wherein the second cache is further configured to communicate  
7 data with the second stencil buffer.

1           5.       The apparatus of claim 4, further comprising a plurality of subtiles,  
2 wherein each tile is divided into a plurality subtiles, wherein the stencil shadow volume  
3 data stored in the first stencil buffer record comprises:

4           a reference value for each of the plurality of subtiles;

5           a delta value for each pixel comprised in the group of pixels; and

6           a plurality of subtile status flags.

1           6.       The apparatus of claim 5, further comprising a FIFO hardware structure,  
2 wherein the FIFO hardware structure is configured to store the first stencil buffer record.

1           7.       The apparatus of claim 5, wherein the plurality of subtile status flags  
2       comprise a plurality of subtile dirty flags, a plurality of subtile overflow flags and a  
3       plurality of subtile underflow flags, wherein there is one of the plurality of subtile dirty  
4       flags corresponding to each one of the plurality of subtiles; wherein there is one of the  
5       plurality of subtile overflow flags corresponding to each one of the plurality of subtiles;  
6       wherein there is one of the plurality of subtile underflow flags corresponding to each one  
7       of the plurality of subtiles.

1           8.       The apparatus of claim 4, wherein the plurality of stencil buffers resides  
2       within any of a plurality of hardware memory structures.

1           9.       The apparatus of claim 4, wherein the plurality of depth buffers resides  
2       within any of a plurality of hardware memory structures.

1           10.      The apparatus of claim 4, wherein the plurality of data caches is located on  
2       a computer graphics processor.

1           11.     A method for generating a shadow effect in a computer graphics system,  
2 comprising the steps of:

3           rendering an object with diffuse color;  
4           generating pixel depth information for a scene for storage in a pixel depth buffer;  
5           generating depth information for a group of pixels, wherein the depth information  
6 for the group of pixel is stored in a compressed depth buffer;  
7           testing the depth information in the compressed depth buffer to determine if the  
8 group of pixel may utilize a shadow mask data in a compressed stencil buffer;  
9           generating the shadow mask data; wherein a first portion of the shadow mask data  
10 is generated in the compressed stencil buffer, wherein a second portion of the shadow  
11 mask data is generated in a pixel stencil buffer;  
12           generating a shadow area, wherein the shadow area is determined by the shadow  
13 mask data contained in the compressed stencil buffer and the pixel stencil buffer; and  
14           adding specular color to objects not in the shadow area.

1           12.     The method of claim 11, further comprising the step of:  
2           generating a shadow volume, wherein the shadow volume comprises a plurality of  
3 front-facing polygons relative to a viewpoint, wherein the shadow volume further  
4 comprises a plurality of back-facing polygons relative to the viewpoint.

1           13.     The method of claim 12, further comprising the step of selectively  
2 incrementing a subtile reference value.

1           14.     The method of claim 13, further comprising the step of selectively  
2 decrementing the subtile reference value.

1           15.     The method of claim 14, wherein the group of pixels is a tile.

1           16.     The method of claim 14, wherein the group of pixels is a subtile.

1           17.     The method of claim 14, further comprising the step setting a plurality of  
2     status flags in the compressed stencil buffer, wherein the plurality of status flags are set to  
3     indicate that a portion of the shadow mask data in the compressed stencil buffer is  
4     incomplete.

1           18.     The method of claim 17, further comprising the step of selectively  
2     merging the shadow mask data in the compressed stencil buffer into the pixel stencil  
3     buffer; wherein the states of the plurality of status flags are utilized to select which  
4     shadow mask data from the compressed stencil buffer is merged into the pixel stencil  
5     buffer.

1           19.     A computer graphics system comprising:  
2     depth data compression logic configured to generate a compressed depth data,  
3     where the compressed depth data corresponds to a group of pixels;  
4     shadow data compression logic configured to generate a compressed stencil  
5     shadow data, where the compressed stencil shadow data corresponds to the group of  
6     pixels, wherein the compressed stencil shadow data is generated utilizing a stencil  
7     shadow volume method;  
8     shadow data generation logic configured to generate an uncompressed stencil  
9     shadow data, wherein the uncompressed stencil shadow data is generated utilizing the  
10    stencil shadow volume method; and  
11    shadow data merging logic configured to selectively merge the compressed stencil  
12    shadow data with the uncompressed stencil shadow volume data.

1           20.     The shadow data generation logic of claim 19, further configured to  
2     selectively generate the uncompressed stencil shadow data, wherein the uncompressed  
3     data is selectively generated based on the compressed stencil shadow data exceeding a  
4     range, wherein the range is determined by a format of the compressed stencil shadow  
5     data.

1           21.     The shadow data merging logic of claim 20, further configured to  
2     selectively merge the compressed stencil shadow data and the uncompressed stencil  
3     shadow data, wherein the merge operation is determined by the state of a plurality of data  
4     status flags.

1           22.     The shadow data merging logic of claim 21, wherein one of the plurality of  
2     data status flags comprises a subtile underflow flag.

1           23.     The shadow data merging logic of claim 21, wherein one of the plurality of  
2     data status flags comprises a subtile overflow flag.

1           24.     The shadow data merging logic of claim 21, wherein one of the plurality of  
2     data status flags comprises a subtile dirty flag.

1           25.     Computer graphics hardware, comprising a means for creating a shadow  
2     effect using a compressed stencil buffer.

1           26.     The computer graphics hardware of claim 25, further comprising:  
2     means for selectively merging shadow mask data for a tile into a pixel stencil  
3     buffer, wherein the tile corresponds to a record in the compressed stencil buffer; wherein  
4     the tile is comprised of a group of pixels; wherein a subtile is comprised of a subset of the  
5     group of pixels.

1           27.     The computer graphics hardware of claim 26, further comprising:  
2     means for storing a pixel depth data in a pixel depth data buffer; and  
3     means for storing a compressed depth data in a compressed depth data buffer,  
4     wherein the compressed depth data corresponds to the tile.

1           28.     The computer graphics hardware of claim 27, further comprising a means  
2     for determining which pixels are in a shadow.

1           29.    The computer graphics hardware of claim 28, wherein the means for  
2   determining which pixels are in a shadow comprises selectively performing a depth data  
3   test on compressed depth data and pixel depth data, wherein the means for determining  
4   which pixels are in a shadow further comprises selectively performing a stencil value not  
5   equal to zero test on pixel stencil data and compressed stencil data.

1           30.    The computer graphics hardware of claim 29, further comprising a means  
2   for adding specular color to pixels not contained in the shadow.